



Attorney Docket No. 35640/36899

BARNES & THORNBURG CUSTOMER NO:

**23646**

U.S. PATENT AND TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE **NOV 23 2004**

Applicant(s): Matsumoto Toshiyuki et al. Conf. No.: 2544  
Serial No.: 09/703,845 Art Unit: 2829  
Filed: November 2, 2000 Examiner: Nguyen, Tung X.  
For: CAPACITANCE MEASUREMENT METHOD OF MICRO  
STRUCTURES OF INTEGRATED CIRCUITS

Fee  
only

**AMENDMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the official Office Action dated May 25, 2004, please amend the above-identified application as follows:

**IN THE CLAIMS**

Please see the Claim Summary Document attached hereto.

**REMARKS**

In response to the official Office Action dated May 25, 2004, Applicant provides the following remarks.

With respect to the objection of the drawings under 37 C.F.R. § 1.83(a) and the rejection of Claim 2 under 35 U.S.C. § 112, the third terminals are the guard terminals  $T_G$  shown in various figures. In Figure 12, the two guard terminals  $T_G$  are  $C_{bb2}$  and  $C_{bj}$ . In Figure 19, the two guard terminals  $T_G$  are  $C_{bp}$  and  $C_{bj}$ . In Figure 19, the guard terminals  $T_G$  are  $C_{wp}$  and  $C_{wg}$ . In Figure 22, the guard terminals  $T_G$  are elements 104 and 106. Thus, there is sufficient support in the drawings for a plurality of third terminals.

The allowance of Claims 20-22 is hereby acknowledged. The objection to Claims 3-5, 8 and 11-19 as being directed to allowable subject matter is also acknowledged.

Objected to Claim 4 has been rewritten as an independent claim. Basically, the preamble of Claim 1 has been inserted, and the redundant parts from Claim 1 have not been included. Thus, Claim 4 is considered allowable.